R09

Code No: D5504

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II - Semester Examinations, March 2011
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(EMBEDDED SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
- - -

1. a) Distinguish among ROM, PLA, PAL.
   b) Describe the salient features of Cypres FLASH 370 Device technology. [12]

2. a) Describe the speed performance and in system programmability of Lattice PLST's architectures in 3000 series.
   b) Draw and explain logic blocks of FPGAs. [12]

3. a) Explain the design structure of AT&Ts optimized reconfigurable cell arrays.
   b) Discuss about the technology mapping for FPGAs. [12]

4. a) Explain one-hot state machine design method.
   b) Describe the extended petrinetes for parallel controllers. [12]

5. a) Give the design flow for parallel adders and parallel controllers using mentor graphics EDA tool.
   b) Define and explain Meta stability in FSMs. [12]

6. a) List out the salient features of mentor graphics EDA tool " FPGA ADVANTAGE".
   b) Discuss about front end digital design tools for FPGAs and ASICs. [12]

7. a) Explain about Linked state machines.
   b) Discuss about the speed performance of ACTEL ACT1, 2, 3. [12]

8. Write any **two** of the following:
   i) Features of Altera FLEX logic-1000 SERIES CPLD.
   ii) ROM
   iii) Applications of CPLD &FPGAs in digital design. [12]

*****